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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/487,004	01/19/2000	TSUTOMU YAMADA		2602

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EXAMINER	
ABRAHAM, FETSUM	
ART UNIT	**PAPER NUMBER**
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/487,004	Applicant(s) YAMADA, TSUTOMU
	Examiner Fetsum Abraham	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-11 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claims rejection

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the submitted prior art in Figure 1.**

As for claim 1, the figure discloses an electroluminescence display device comprising a light emissive element (163) provided between first anode electrode (161) and second cathode electrode (162), a first double gated TFT (130) receiving a selection signal at its gate from a scan driver not shown in the figure via gate wire (Gn) to acquire data signal through data line Dm driven by data driver not shown in the figure, a second TFT (143) between driving power line (150) and the emissive element (163), and controlling power supplied through the power line in accordance with the switching data signal from the first transistor via the gate line (141), but all device elements such as the conductivity types of the transistors, whether they have LDD structures and if they were offset transistors. However, device conductivity type does not alter the basic similarity of NMOSFETs and PMOSFETs, since their most significant difference is known to be applied voltage polarities, while LDD elements are commercially available because of their superior hot carrier prevention characteristics. Therefore, it would have been obvious to one

skilled in the art to utilize any conductivity type LDD based transistors for the reasons mentioned above.

As for said offset type transistors in the claim, all TFTs at least have gates vertically offset from the active layers by a width equal to the width of the gate insulation layers.

As for claims 2,3, TFTs with non-single crystalline, and specifically polycrystalline materials are known in the art and commercially available in the art. Therefore, it would have been obvious to one skilled in the art to use a crystallized active TFT layers since such layer have better conductance and superior mobility characteristics compared to regular silicon based TFTs.

As for claim 4, there are only two main types of transisors in the art: top or bottom gate transistors. Therefore, it is clear that the prior art utilizes one of the types.

As for claim 5, the similar to the claimed elements in the structure form a pixel in the display matrix.

As for claim 6, the claimed arrangement is the most basic one in display arrays. The elements must be arranged according to the claimed arrangement for all display arrays to function properly. The structure can also be seen in the figure.

As for claim 7, the capacitor of the device is located between the claimed elements of figure 1.Please note that crystallized active layers in TFTs include the sources, the drains, and the channels of the same.

As for claim 8, the optical element is a non organic optical device.

As for claim 9, the first transistor is a multigated device with a drain region connected to drain line (132) and source region (133) connected to a storage capacitor (142).. In the array, the second transistor (143) has its drain connected to a driving power supply line (150) and the gate to the source (133) of the first transistor. Although there is no complete information about the prior art concerning LDD, offset characteristics and the conductivity type of the transistors, the issues have been declared to be well known in the art as discussed above.

As for claims 10,11, the element (163) of the display matrix is light emissive.

3. **Claims 1-6,8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani (6,277,679).**

As for claim 1, Ohtani discloses an electroluminescence device in figure 15B comprising a light emissive element (3505) provided between first anode electrode and second cathode electrode, a first double gated TFT (3502) receiving a selection signal at its gate from a scan driver not shown in the figure via gate wire (38) to acquire data signal through the source line driven by data driver not shown in the figure, a second TFT (3503) between driving power line (3506) and the emissive element (3505), and controlling the power supplied through the power line (3506) in accordance with the switching data signal from the first transistor via the gate line of transistor (3503). The patent clearly teaches about the application of LDD based offset TFTs (see column 2, 45-50) but the exact conductivity types of the transistors is not clearly stated. However, NMOSFETs and PMOSFETs are exchangeable elements in the art because of the above addressed minor differences.

As for claims 2,3, TFTs with non-single crystalline, and specifically polycrystalline materials are known in the art and commercially available. Therefore, it would have been obvious to one skilled in the art to use a crystallized active TFT layers since such layer have better conductance and superior mobility characteristics thereby increased device speed compared to regular silicon based TFTs.

As for claim 4, there are only two main types of transisors in the art: top or bottom gate transistors. Therefore, it is clear that the prior art utilizes one of the types (see column 2, 45-50).

As for claim 5, the two switching transistors (3502) and the sensor (3505) and the storage capacitor (3504) make up one pixel in the matrix of the display matrix in the patent.

As for claim 6, the claimed arrangement is the only and most basic assembly of elements in any display array to function properly. This includes the display matrix of the prior art (see fig. 15B).

As for claim 8, the optical element is a non organic optical device.

As for claim 9, the first transistor is a multigated device with a drain region connected to drain line (132) and source region (133) connected to a storage capacitor (142). In the array, the second transistor (143) has its drain connected to a driving power supply line (150) and the gate to the source (133) of the first transistor. The patent clearly teaches about the application of LDD based offset TFTs (see column 2, 45-50) but the exact conductivity types of the transistors is not clearly stated. However, NMOSFETs and PMOSFETs are exchangeable elements in the art because of the above addressed minor differences.

As for claims 10,11, the element (163) of the display matrix is light emissive.

Any inquiry concerning this communication should be directed to Fetsum Abraham at telephone number (703) 305,3793, or by E-mail at ***fetsum.abraham@uspto.gov.***

Any inquiry of a general nature or relating to the status of this application should be directed to the ***SPE of AU***:2826 at (703)308-6601, or the ***Group receptionist*** at (703) 308-0956.

Fetsum Abraham

2/12/02